REMARKS

This Response responds to the Office Action dated July 22, 2005 in which the Examiner objected to claim 14 and rejected claims 1-14 under 35 U.S.C. §102(a).

Applicant respectfully points out to the Examiner that although priority has been acknowledged, applicant believes that Box 12a1. should be checked rather than box 12a2. Applicant respectfully requests the Examiner corrects the acknowledgment of priority.

Applicant respectfully points out to the Examiner that claim 14 is not a duplicate of claim 1. In particular, claim 1 claims intra-block output stage sequential circuit**s** while claim 14 claims an intra-block input stage sequential circuit. Additionally, claim 1 claims intra-block output stage sequential circuit**s** while claim 14 claims an intra-block output stage sequential circuit. Also, claim 1 claims extra-block input stage sequential circuit**s** while claim 14 claims an extra-block input stage sequential circuit. Additional features are also distinguished between claims 1 and 14 by claim 1 claiming a plurality of objects while claim 14 claims a single object. Since claim 14 is distinguished from claim 1, applicant respectfully requests the Examiner withdraws the objection thereto.

Claims 1-14 were rejected under 35 U.S.C. §102(a) as being anticipated by Synopsys Design Compiler Tools (http://web.archive.org/web/20020814203544 /http://www.synopsys.com/products/logic/design_compiler.html).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §102(a). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

The *Synopsys* website merely gives a general description of its compiler called DC Ultra. Nothing on the website shows, teaches or suggests the details of the DC Ultra compiler or how it functions. In particular, when 'timing optimization' is clicked on the website, it merely indicates that DC Ultra performs timing optimization. Similarly, when 'data path optimization' is clicked, it merely indicates that the DC Ultra Module Compiler performs this function. Also, when 'power optimization' is clicked, an indication that the Power Compiler will perform this feature. Nothing on the website shows, teaches or suggests any detailed features. In particular, nothing on the website shows, teaches or suggests a) an input/output information identifying unit for identifying intra-block input stage sequential circuit(s) and intra-block output stage sequential circuit(s) by comparing logical connection information with a library, the intra-block input stage sequential circuit(s) are placed in a functional block and contributes to information exchange with extra-block input stage sequential circuit(s) outside the functional block through input pin(s), the intra-block output stage sequential circuit(s) are placed in the functional block and contribute to information exchange with extra-block output stage sequential circuit(s) outside the function information describing connection relationships between circuit components constituting the functional block, between the circuit components and the input pins and between the circuit components and the output pin(s), b) a delay time calculating unit for calculating first delay time(s) from the input pin(s) to the intra-block input stage sequential circuit(s) and second delay time(s) from the intra-block output stage sequential circuit(s) to output pin(s) and c) a timing information output circuit as claimed in claims 1 and 14. Rather, the *Synopsys* website merely discloses general information about its products and how they can be used.

Applicants respectfully point out to the Examiner that the present invention is directed to modeling which is carried out when a design is not yet completed, while *Synopsys* is a tool for design in itself. In other words, the present invention and *Synopsys* are very different from one another.

Since *Synopsys* is directed to a different invention than claims 1 and 14 and since nothing in the *Synopsys* website shows, teaches or suggests the detailed features as claimed in claims 1 and 14, applicant respectfully requests the Examiner withdraws the rejection to claims 1 and 14 under 35 U.S.C. §102(a).

Claims 2-13 depend from claim 1 and recite additional features. Applicant respectfully submits that claims 2-13 would not have been anticipated by the *Synopsys* website within the meaning of 35 U.S.C. §102(a) at least for the reasons as set forth above. Therefore, applicant respectfully requests the Examiner withdraws the rejection to claims 2-14 under 35 U.S.C. §102(a).

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL PC

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